Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A clock based voltage deviation detector comprising:

a pulse module having a pulse input for receiving a clock signal and a pulse output for outputting a stream of reset pulses, wherein said pulse module includes,

a delay cell having a first delay input for receiving said clock signal and a delay output for outputting a delayed clock signal as a function of said clock signal; and

an exclusive-OR gate having a first exclusive-OR input for receiving said clock signal, a second exclusive-OR input communicatively coupled to said delay output of said delay cell and an exclusive-OR output for outputting said stream of reset pulses as a function of said clock signal and said delayed clock signal;

an indicator module having a first indicator input for receiving an input signal, a second indicator input for receiving a reference voltage, a third indicator input communicatively coupled to said pulse output of said pulse module and an indicator output for outputting a pass/fail indicator signal as a function of said stream of reset pulses and a difference between said input signal and said reference voltage; and

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a correlation module having a first correlation input for receiving said clock signal, a second correlation input communicatively coupled to said indicator output of said indicator module, wherein an event of said pass/fail indicator signal is correlated to a specific period of said clock signal at which said event occurred.

2. (Canceled).

3. (Original) The clock based voltage deviation detector according to Claim 1, wherein said correlation module comprises:

a counter having a counter input for receiving said clock signal and a counter output for outputting a count value as a function of said clock signal; and

a storage module having a first storage input communicatively coupled to said counter output and a second storage input for receiving said pass/fail indicator, wherein said count value corresponding to said event of said paid/fail indicator is stored.

4. (Original) The clock based voltage deviation detector according to Claim 1, wherein said indicator module comprises:

a comparator having a first comparator input for receiving said input signal, a second comparator input for receiving said reference voltage and a comparator output for outputting a trip signal as a function of a difference between said input signal and said reference voltage; and

a latch having a first input communicatively coupled to said comparator output of said comparator, a second input communicatively coupled to said pulse output and a latch output for outputting said pass/fail indicator as a function of said trip signal and said stream of reset pulses.

5. (Currently Amended) The clock based voltage deviation detector according to Claim 1, wherein said indicator module comprises a latch-enabled comparator having a first comparator input for receiving said input signal, a second comparator input for receiving said reference voltage, a third comparator input communicatively coupled to said pulse output of said pulse module and a comparator output for outputting said pass/fail indicator signal as a function of said stream of reset pulses and a difference between said input signal and said reference voltage.

6-9. (Canceled).

10. (Original) A clock based voltage deviation detector comprising:

a pulse module for generating a stream of reset pulses as a function of a clock signal;

an indicator module for generating a pass/fail indicator signal as a function of said stream of reset pulses and a difference between an input voltage and a reference voltage;

a counter for generating a count value as a function of said clock signal; and

a storage module for saving a particular count value at which an event of said pass/fail signal occurs.

11. (Original) The clock based voltage deviation detector according to Claim 10, wherein said pulse module comprises:

an OR gate having an OR gate input for receiving said clock signal; and

an exclusive-OR gate having first input for receiving said clock signal, a second input communicatively coupled to an OR gate output of said OR gate, and an output for outputting said stream of reset pulses.

12. (Original) The clock based voltage deviation detector according to Claim 11, wherein said indicator module comprises a latch-enabled comparator having a first comparator input for receiving said input voltage a second comparator input for receiving said reference voltage, a third comparator input for receiving said stream of reset pulses, and a comparator output for outputting said pass/fail indicator signal.

13. (Original) The clock based voltage deviation detector according to Claim 12, wherein:

said first comparator input of said latch-enabled comparator comprises a non-inverting input;

said second comparator input of said latch-enabled comparator comprises an inverting input;

said third comparator input of said latch-enabled comparator comprises a latch enable input; and

said event comprises an overvoltage.

14. (Original) The clock based voltage deviation detector according to Claim 12, wherein:

said first comparator input of said latch-enabled comparator comprises an inverting input;

said second comparator input of said latch-enabled comparator comprises a non-inverting input;

said third comparator input of said latch-enabled comparator comprises a latch enable input; and

said event comprises an undervoltage.

15-17. (Canceled).

18. (Currently Amended) A clock based voltage deviation detector comprising:

a means for generating a reset pulse stream as a function of a clock signal;

a means for generating a delayed reset pulse stream as a function of said clock signal;

a means for generating a pass/fail indicator signal as a function of said reset pulse stream, said delayed reset pulse stream and an event of a monitored voltage; and

a means for correlating an event of said pass/fail indicator signal with a specific period of said clock signal at which said event occurred.

19. (Canceled).

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20. (Currently Amended) The clock based voltage deviation detector according to Claim 18, wherein said means for generating a pass/fail indicator signal comprises:

a means for detecting said event of said monitored voltage and generating a first trip signal until receipt of a next pulse of said reset pulse stream;

a means for detecting said event of said monitored voltage and generating a second trip signal until receipt of a next pulse of said delayed reset pulse stream; and

a means for generating said pass/fail indicator signal as a function of said first trip signal and said second trip signal.

21. (New) The clock based voltage deviation detector according to Claim 18, wherein said monitored voltage comprises an input voltage relative to a reference voltage.